Hardware implementation of linear algebra operators for small floating point formats

Orégane Desrentes

- **Kalray**
- **2** Floating point linear algebra
- ³ 8 bits formats

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A complete offer or data-intensive applications

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Two application domains:

Data Center acceleration Computing

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- Compression and decompression
- Encryption and decryption
- Erasure coding
- De-duplication

Computing

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Computing

- Machine Learning
- Computer vision
- Pre/post processing
- Signal processing

Kalray MPPA® scalable many-core architecture

3rd-gen MPPA® processor: in TSMC 16nm technology, up to 1.2 GHz

Multiple Processors per Card

MPPA3 V2 Coolidge™ processing element (PE)

6-issue 64-bit VLIW core with a tightly-coupled tensor coprocessor **VLIW Core**

- Scalar 32-bit and 64-bit INT & FP
- 8 \times 8-bit, 4 \times 16-bit, 2 \times 32-bit SIMD
- 128-bit 256-bit SIMD operations by bundling multiple instructions
- 256-bit load/store unit with masking

Tensor Coprocessor

- Matrix multiply-add on 4×4 tiles
- 512-bit multiply and add operands
- Matrix zip/unzip & transpose
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Coprocessor collective tensor operations

- PE operation: INT8.32 $(4 \times 16) \cdot (16 \times 4)$ $+ = (4 \times 4)$
- Macro-scheme executed by 4 PEs
	- 8×256 -bit memory loads (XLO) per PE
	- 8 \times 256-bit data exchanges per PE
	- $8\times$ matrix multiply-add operations per PE
- Matrix A and B are loaded by quarter by each PE which exchange one quarter with 2 different PFs
- Kernel for INT8.32: $(16 \times 32) \cdot (32 \times 16) + (16 \times 16)$

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Coprocessor Matrix multiply-accumulate operations

8-bit to 32-bit int matrix multiply-add: (4×16) int8 (16×4) int8+ = (4×4) int32 16-bit to 32-bit FP matrix multiply-add: (4×8) FP16 (8×4) FP16+ = (4×4) FP32 **Signature**

- 512 -bit \times 512-bit $+=$ 512-bit
- 256-bit register-pair multiplicands
- 256-bit register-pair accumulator

Performances

- 256 MADD eq. per cycle, 512 ops/c
- 128 FMA eq. per cycle, 256 flops/c
- 50 TOPS @1.2 GHz for 80 cores
- 25 TFLOPS @1.2 GHz for 80 core

[Floating point linear algebra](#page-11-0)

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For floats: $w_S = 1$, $w_F = 8$, $w_F = 23$

• $+0, -0$

- $+0, -0$
	- \bullet *S* = sign
	- $E = 0$
	- $F = 0$

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Why we need them

Avoid numbers being flushed to 0 abruptly: gradual underflow. Guarantees if $x \neq y$ then $x - y \neq 0$ and other useful properties.

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Why they are annoying

They have less precision than w_F . They are encoded differently: $(-1)^S \times 2^E \times 0. P$ Where the first significant bit ? $0.F = 0.000000011001100$

 \Rightarrow They used to be treated in micro-code but now we do subnormal hardware

Short and biased history of floating point units

• In the 70s, adders and multipliers

$$
\bullet \ \ R = \circ (X + Y)
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	- two operations in one instruction: *faster*
	- one single rounding: *more accurate*

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Multiple applications

- Matrix multiplication (neural networks, graphical applications, scientific computing, ...)
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Objective: better than FMA chains

$$
Z + \sum_{i=0}^{N-1} X_i \times Y_i \approx \circ (\ldots \circ (\circ (Z + X_0 \times Y_0) + X_1 \times Y_1) \ldots + X_N \times Y_N)) \mathbb{D}
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Easy, but the result is not a IEEE-754 floating point number:

- Not rounded
- Signed significands
- Significands are not normalised
	- Float is in $[1, 2]$ but product is in $[1, 4]$
	- **Product of normal and subnormal**

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If exactly in the middle, round to an even float.

 \Rightarrow We need the following information to round:

3.141592654 goes in $\circ(\pi)|$ boolean information: is this 0 ? "sticky bit"

boolean information: is this digit over or under 5 ? "round bit"

Sum of floating point numbers

Rounding the sum of two floating point numbers

We sort (E_0, M_0) , (E_1, M_1) such that $E_0 \ge E_1$

Sum like integers

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*M*₁ is completely compressed in a "sticky bit"

Rounding the sum of more than two floating point numbers - problem !!

Problem: cancellation

 $M_0 = -M_1$ and $E_0 \gg E_2$ $M_0 + M_1 + M_2 = M_2$ If *M*₂ has been totally compressed in a sticky bit, we cannot retrieve the result.

Problem: multi-sticky

 $E_0 \gg E_1$ and $E_0 \gg E_2$ If M_1 et M_2 were compressed, we cannot round the result M_0

- Method:
	- Convert to fixpoint
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Kulisch accumulator: Architecture

Size in bits for FP32 dot-product

Kulisch accumulator: Expensive and empty

A less expensive version: truncated Kulisch

- Method similar to floating point sum:
	- Choose $w_{\text{acc}} < w_{\text{full}}$ (arbitrarily)
	- Align all numbers on the biggest one, throw away any bits that don't fill in W_{acc} (no sticky, we don't care)
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	- Sum like integer, round to float
- Inexact computation

Truncated Kulisch accumulator: Architecture

TC.

Correctly rounded sum of products

 1 O. Desrentes, B. Dupont de Dinechin, F. de Dinechin, "Exact Fused Dot Product Ω Add Operators"

Correctly rounded sum of products

Architecture comparison

Kulisch

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*w*full ∼ 2 *w^E w*compressed ∼ *N* × *w^F*

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3 situations:

• The format has a lot of precision compared to the range, $W_{\text{compressed}} > W_{\text{full}}$ even for small *N*

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*w*full ∼ 2 *w^E W*_{compressed $∼$ *N* $×$ *W_F*}

3 situations:

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- The format is more balanced, $w_{\text{compressed}} < w_{\text{full}}$ for small *N*
- The format has a lot of range compared to the precision *w*compressed < *w*full until larger *N*

[8 bits formats](#page-105-0)

Formats

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 $\mathbf R$
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8 bits is not a lot of bits (256 different values)

C.4 Value Table: P4, $P = 4$, emax = 7

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NaN

Having 2^{w_F+1} – 2 NaN values is a waste of encoding space. Should we keep at least one ? Yes

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−0

Having 2 zeros is a waste of encoding space. Should we keep −0 ? Maybe

IEEE-754-like:

Graphcore¹:

¹B. Noune, P. Jones, D. Justus, D. Masters, and C. Luschi, "8-bit numerical formats" for deep neural networks," 2022

Intel Arm NVIDIA²:

²P. Micikevicius, D. Stosic, N. Burgess, M. Cornea, P. Dubey, R. Grisenthwaite, S. Ha, A. Heinecke, P. Judd, J. Kamalu, N. Mellempudi, S. Oberman, M. Shoeybi, M. Siu \blacksquare and H. Wu, "Fp8 formats for deep learning," 2022

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IEEE WG P3109 standard 3 :

3 "IEEE Working Group P3109 Interim Report on 8-bit Binary Floating-point Formats"

IEEE WG P3109 standard (with saturation) 3 :

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For a real exponent E, it is encoded in the format like a positive number, by adding a bias.

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Block floating point

History

A vector of fixpoint numbers that share an exponent.

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Recent variant

A vector of small floating point numbers that share a bias modifier/scaling factor

Kulisch architecture for exact 8 bits dot product

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Comparison with other 8 bits formats: posits and integers

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How it is implemented in the MPPA

Instead of accumulating in large fixpoint, use a FP32

Back to the 70s

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*^a*B. Hickmann and D. Bradford, "Experimental analysis of matrix multiplication functional units", 2019

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*^b*B. Hickmann, J. Chen, M. Rotzin, A. Yang, M. Urbanski, S. Avancha, "Intel Nervana Neural Network Processor-T (NNP-T) Fused Floating Point Many-Term Dot Product", 2020

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*^c*D. Lutz, A. Saini, M. Kroes, T. Elmer, H. Valsaraju, "Fused FP8 4-Way Dot Product with Scaling and FP32 Accumulation", 2024

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- Kalray is continuing the exact Kulisch with rounding by block of 8? products, with E5M2 and E4M3 (but which ones ?)
- IEEE WG P3109 formats are a description of everything that can be done

